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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/069,195	11/07/2002	Gilbert Wolrich	10559-304US1	1605

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EXAMINER	
LAI, VINCENT	
ART UNIT	PAPER NUMBER
2181	
MAIL DATE	DELIVERY MODE
05/14/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/069,195	WOLRICH ET AL.	
	Examiner	Art Unit	
	Vincent Lai	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-17 and 19-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6,9-14,16 and 19-25* is/are rejected.

7)☒ Claim(s) *4,5,7,15 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 26 February 2007 has been entered.

Information Disclosure Statement

2. The information disclosure statements (IDS) submitted on 26 February and 1 May 2007 have been being considered by the examiner.

Allowable Subject Matter

3. The indicated allowability of claims 1-7, 9-17, and 19-25 is withdrawn in view of the newly discovered reference(s) to Kane (PA-RISC 2.0 Architecture). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3, 6, 9-14, 16, and 19-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Kane (PA-RISC 2.0 Architecture), herein referred to as Kane.

As per **claim 1**, Kane discloses a computer program product residing on a computer readable storage medium comprising instructions (See page 7-13: The reference is teaching an instruction), including a branch instruction (See page 7-13: The reference is teaching a specific type of branch instruction) that when executed on a computing device causes the computing device to:

cause an instruction stream to branch to another instruction in the instruction stream to branch to another instruction based on a bit of a register being set or cleared (See page 7-13: Purpose of the branch on bit instruction), the branch instruction specifying the register (See page 7-13: r is the specified register in the instruction) and the bit of the register to use as a branch control bit (See page 7-13: pos specifies the position of the bit which determines whether to branch or not).

As per **claim 2**, Kane discloses wherein the branch instruction comprises

a bit_position field that specifies the bit position of the branch control bit in a longword contained in a register (See page 7-13: pos is the bit-position of the instruction).

As per **claim 3**, Kane discloses wherein the branch instruction comprises

a branch target field specified as a label in the instruction (See page 7-13: One of the instruction fields is a target).

As per **claim 6**, Kane discloses wherein the register is a context-relative transfer register or a general-purpose register that holds the operand (See page 7-13: The description described register r as being a general register (GR)).

As per **claim 9**, Kane discloses wherein the branch instruction allows a programmer to select which bit of the register to used to determine the branch operation (See page 7-13: The bit to be used is determined with the pos value).

As per **claim 10**, Kane discloses wherein the branch instruction allows branches to occur based on evaluation of a bit that is in a data path of a processor (See page 7-13: Branches are done after evaluating the specified bit in a register).

As per **claim 11**, Kane discloses a method of operating a processor comprises:

evaluating a specified bit of a specified register designated to use as a branch control bit (See page 7-13: Branches are done after evaluating the specified bit in a register); and

performing a branching operation based on the specified bit of the specified register being set or cleared (See page 7-13: In the case of a single bit being used as the branch condition, the specified would be have to be either set or cleared).

As per **claim 12**, Kane discloses wherein the specified bit position is in a longword contained in a register (See page 7-13: pos is the bit-position of the instruction).

As per **claim 13**, Kane discloses further comprising:

branching to an instruction at a branch target field specified as a label in the instruction (See page 7-13: One of the instruction fields is a target).

As per **claim 14**, Kane discloses wherein the specified bit is specified by a programmer (See page 7-13: The instruction can be set by a programmer such that the bit is chosen by a programmer).

As per **claim 16**, Kane discloses wherein the register is a context-relative transfer register or a general-purpose register that holds the operand (See page 7-13: The description described register r as being a general register (GR)).

As per **claim 19**, Kane discloses wherein the instruction allows a programmer to select which bit of the specified register is used to determine the branch operation (See page 7-13: The bit to be used is determined with the pos value).

As per **claim 20**, Kane discloses wherein branch evaluation occurs based on evaluation of bits that are in a data path of a processor (See page 7-13: Branches are done after evaluating the specified bit in a register).

As per **claim 21**, Kane discloses a processor comprises:

a register stack (See page 1-6: The general registers);

an arithmetic logic unit (See page 1-6: ALU) coupled to the register stack and a program control (See figure 1-6: The program counter and the instruction register comprise the program control) store that stores a branch instruction (See figure 1-6: The instruction register can store branch instructions) that causes the processor to:

evaluate a bit of the registers of the register stack, the bit designated to use as a branch control bit (See page 7-13: Branches are done after evaluating the specified bit in a register); and

perform a branching operation specified by the branch instruction based on the bit of the register being set or cleared (See page 7-13: In the case of a single bit being used as the branch condition, the specified would be have to be either set or cleared).

As per **claim 22**, Kane discloses wherein the specified bit is in a longword in a general purpose register (See page 7-13: pos is the bit-position of the instruction).

As per **claim 23**, Kane discloses further comprising:

a branch target field specified as a label in the instruction (See page 7-13: One of the instruction fields is a target).

As per **claim 24**, Kane discloses wherein the specified bit is specified by a programmer (See page 7-13: The instruction can be set by a programmer such that the bit is chosen by a programmer).

As per **claim 25**, Kane discloses wherein the one of the registers is a context-relative transfer register or a general-purpose register that holds an operand (See page 7-13: The description described register r as being a general register (GR)).

Allowable Subject Matter

5. Claims 4, 5, 7, 15, and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The primary reasons that claims 4, 5, 7, 15, and 17 would be allowable if rewritten is the prior art of record neither anticipates nor renders obvious the combination of the various limitations of the claim itself in conjunction with the following limitation of the independent claims: "the branch instruction specifying the register and the bit of the register to use as a branch control bit."

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent Lai whose telephone number is (571) 272-6749. The examiner can normally be reached on M-F 8:00-5:30 (First BiWeek Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Vincent Lai
Examiner
Art Unit 2181

vl
May 9, 2007

DONALD SPARKS
SUPERVISORY PATENT EXAMINER